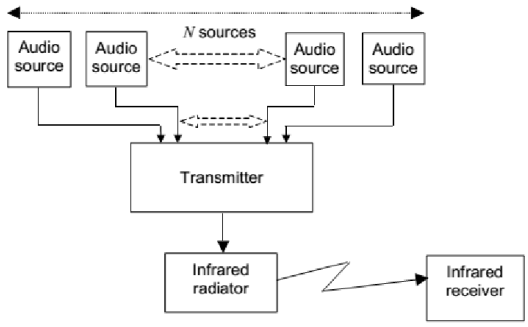
TELECOM

MW_MODEM (D)QPSK Core

General Description

The MW_MODEM (D)QPSK core performs the physical layer for baseband modulator/ demodulator data transmission over point-to-point radio links.
The core included (D)QPSK signal mapping using a look-up table and a square root raised cosine channel filtering to reduce Inter-Symbol Interference (ISI) and spectral spreading.
Square root raised cosine filtering of the I and Q channel streams at the modulator output was implemented digitally using a 97 tap FIR filter and implemented in both the transmitter and the receiver, resulting in a total transfer characteristic of a raised cosine.
A technique called interpolation was used in the filtering algorithm to increase the sampling rate and relax the reconstruction filter design. The output was sampled by the D/A converter.
The baseband bandwidth occupied in each channel is given by (1+α) * Bit rate / 2, with the capability to move from 0.5 MHz to 8 MHz.
A Reed Solomon encoder is included to protect the data information from transmission errors.
MW_MODEM (D)QPSK core was developed in Vivado tool, written in HDL code, and tested on Xilinx Artix™ 7 series and Xilinx Zynq™ FPGA. Structural simulation and hardware test was performed to check compliant with Matlab model. FPGA netlist only or complete design environment package are deliverable.



Features

- (D)QPSK digital modulation/demodulation technology
- Analogue or digital signal sources
- Channel bandwidth : 0.5 to 8 MHz
- Reed Solomon encoding
- SRRC channel filter
- Carrier and timing recovery
- Suitable for various kinds of application halls and outdoor venues
- Low complexity design
- Zynq/Artix7 technology and ISE Xilinx 14.7/ Vivado tool

Application

A particular (D)QPSK modem use is in infrared transmission audio/video systems, for conference interpretation, using the frequency range 2MHz to 7MHz.
The system consists of a number (N) of audio sources, either analogue or digital, which are connected to the transmitter. The transmitter processes the audio signals into an electrical output to feed the infrared radiator. The infrared signal is received by the infrared receiver that processes the signal and outputs an audio signal and/or associated data.

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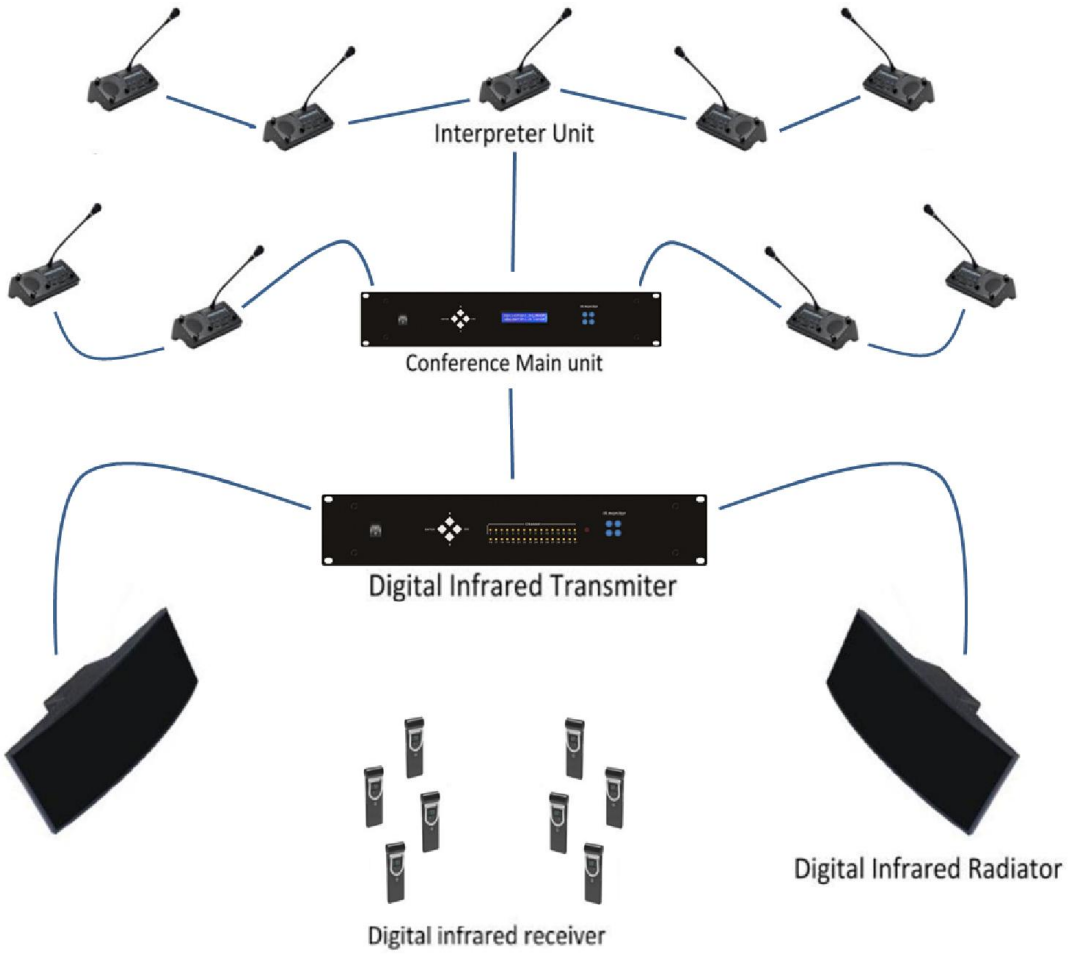

Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:
http://www.mindway-design.com

or send an e-mail at:

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