MW_SPI2TS Core

General Description

The MW_SPI2TS core prevents the processing of malformed TS packets. It mainly stops packets without the appropriate combination of sync pulse and sync byte (0x47) or packets containing less than 188 bytes. It also generates four flow control signals associated with TS flow: 'stop' signal indicates that there is no incoming flow, 'stable' is the logical NOT of previous signal, 'start' is a pulse generated whenever the flow locks after a previous stop and 'length' indicates the type of TS packet (188 or 204 bytes).
SPI (Synchronous Parallel Interface) is a parallel video communication standard defined by the DVB consortium for use in transporting MPEG-encoded video stream. DVB-SPI is frequently used in satellite transmission, interfacility links and telephony communication. DVB-SPI is designed to transport MPEG-2 video streams, primarily for television applications.
Input SPI flow is initially sampled with rising edge of SPI2TS_in_CLK, then resampled to Fast_Clk domain; this way all other core operation does not depends any more on SPI2TS_in_CLK, increasing the core robustness in case of noise environments.
Data are sent to Packet_Framer to delineate TS packets. It has three different operating modes. In START mode, it tries to delineate the flow from scratch. In STABLE mode, it performs continuous monitoring on the flow and, additionally, the bandwidth of the flow is checked. In STOP mode the block waits for a while to provide information to user application that the flow has broken or stopped.
Even if the PACKET_FIFO is only 16 positions, it behaves in 'packet mode' due to clever PACKET_FIFO_CONTROL block. It reads the content of the FIFO and avoids generation of 'wrong length packets' that may occur.
Last, the LED_Ctrl provides information about the status of the Link.
SPI2TS core requires a reference clock that is used for timeouts and all other activities where precise timing is required.
FPGA netlist only or complete design environment package are deliverable.

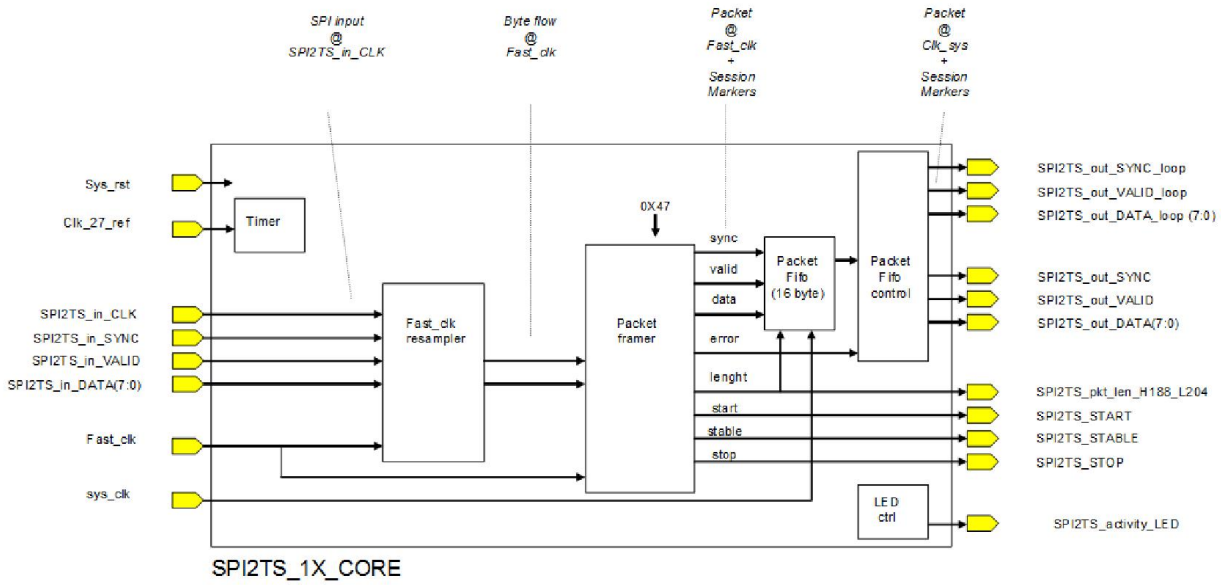
Features

- Standard implementation of DVB-SPI
- Precise and robust design
- Implementation is agnostic with respect to SPI_SYNC and SPI_Clock
- Several instances of the core can be mapped in the same low-cost FPGA
- Validation in Xilinx Zynq device and Xilinx Vivado environment
- Cheapest implementation of complex video broadcasting appliances with no risk of performance tradeoffs
- Input parallel data resampling using local high speed clock, thus increasing noise robustness
- Transport Stream flow synchronization and generation of 'session' flags
- TS flow adaptation to user clock rate
- Hardware protection from transmission errors or mismatch
- LED indication of Active Link and Current Rate
- Inexpensive implementation with reduced FPGA resources

Slices	Slice Reg	LUTs	LUTRAM	BRAM/FIFO	DSP48E1
129	232	259	8	0	0

- Zynq/Artix7 technology and ISE Xilinx 14.7/ Vivado tool

Typical Application



Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:

http://www.mindway-design.com

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