NETWORKING

MW_HPS Core

General Description

The MW_HPS (Hardware IP Protocol Stack) is the perfect solution for conversion of high speed local interfaces (e.g. USB2, IEEE 1394, PCIExpress, ASI-DVB) to Fast/Giga-Ethernet IP for high speed, persistent throughput and low latency applications.
Due to the fact that Software implementation of the IP stack for all these applications is bottlenecked by the processor, MindWay solution is fully hardware-based, overcoming these limits and allowing customers to match whatever throughput requirement.
MW_HPS offers both the Receiver and Transmitter side built around the MAC block. To be compliant with the newest MAC blocks, an AXI Stream Interface is provided to interface with the Rx and Tx Buffer, so it is simpler to embed such a type of core in the design. Each port shall be provided with a specific HW protocol handler (e.g. IP2TS, TS2IP, IPTV, FTP handlers). Each handler shall be configured in order to manage the desired channel.
At the transmitting side data flows are packetized according to the kind of protocol handler, multiplexed with other outcoming packets and then delivered to the network. Packet Multiplexing is prioritized to minimize loss.
At the receiving side, network packets are filtered and delivered to the proper handler that depacketizes them.
Some ports are used internally for protocols requiring automatic answer. To have a real plug-and-play solution that performs the main functions helping in network troubleshooting, the following IPv4/IPv6 protocols are supported: ARP, ICMP, ICMPv6 NDP and ICMv6 ECHO. With these protocols the consistency of the link can be immediately asserted.
There are also dedicated ports that can bridge standard processor architecture, e.g. based on inexpensive Microblaze™, where a standard software IP stack is implemented.
External Ethernet PHY devices can be configured (via MDIO interface) by means of dedicated EMAC_MII Hardware configurator.
FPGA netlist only or complete design environment package are deliverable.

Features

- Fully-hardware implementation of the standard IP stack avoids the need of extra software development and resulting bottlenecks
- It supports any appliance requiring conversion of data to IP and vice versa
- Transport Streams video flows can be easily adapted to IP transportation
- MindWay provides a complete ecosystem of available Cores that allow you to build lots of IP-based video applications
- Multiple instances of MW_HPS in a single FPGA permit to easily implement networking functionalities (bridging and routing, HW servers, protocol adapters, etc.), dramatically reducing design complexity and costs
- Inexpensive implementation with reduced FPGA resources (the limited size of the core leaves enough space for other complex functions, such as modulator, data compressors, crypto engines, etc.)

Slices	Slice Reg	LUTs	LUTRAM	BRAM/FIFO	DSP48E1
1407	3346	4063	342	2	0

- Validation in Xilinx Artix device and Xilinx ISE environment

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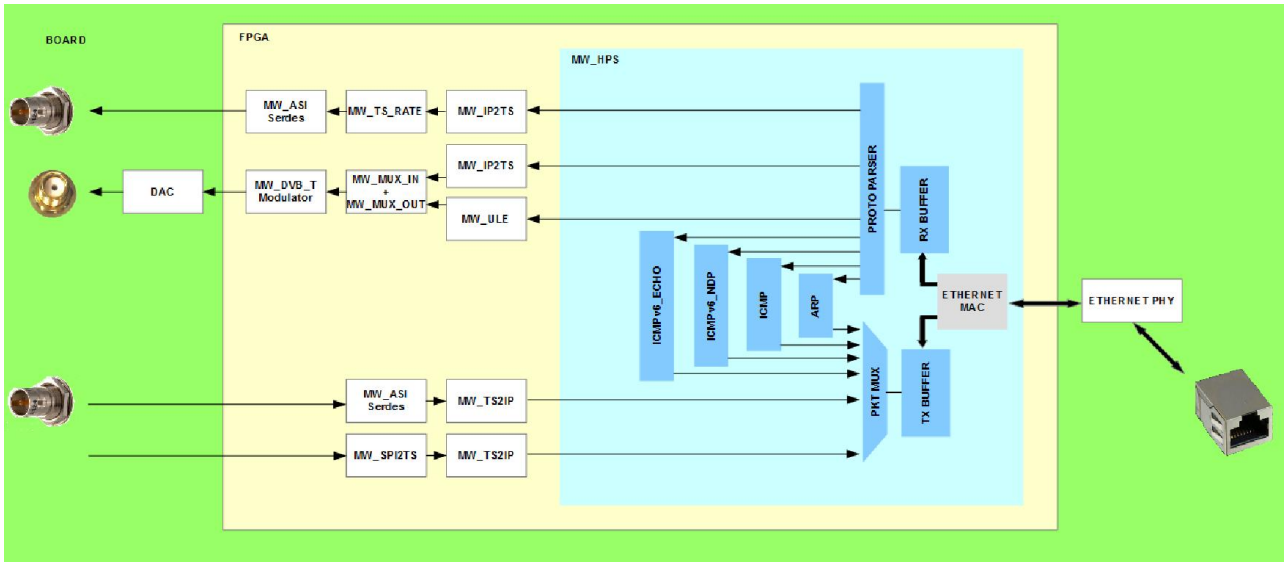
Architecture and Typical Application



Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx 7 Series technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE/Vivado constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:

http://www.mindway-design.com

or send an e-mail at:

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