PIANIFICAZIONE TRAINING XILINX Q4 2012

Data (*)	Durata	Corso	Costo	TC
2 -3	2	Designing with the Spartan-6 Families	€ 1600 + IVA	18
9 - 10	2	Design for Performance	€ 1600 + IVA	18
11 - 12	2	Minimizing Your Design Time with the ChipScope Pro Debug and Verification Tools	€ 1600 + IVA	18
16-17-18	3	Designing with VHDL	€ 1800 + IVA	21
22 - 23	2	Embedded Systems Development	€ 1600 + IVA	18
29 - 30	2	DSP Design Using System Generator	€ 1600 + IVA	18

Ottobre 2012

L	M	M	G	V	S	D
1	**2**	**3**	4	5	6	7
8	**9**	**10**	**11**	**12**	13	14
15	**16**	**17**	**18**	19	20	21
22	**23**	24	25	26	27	28
29	**30**	31				

Data (*)	Durata	Corso	Costo	TC
6 - 7	2	Advanced FPGA Implementation	€ 1600 + IVA	18
12	1	Essentials of FPGA Design	€ 800 + IVA	9
15 - 16	2	Advanced Design with the PlanAhead Analysis and Design Tool	€ 1600 + IVA	18
19 - 20	2	Zynq EPP System Architecture	€ 1600 + IVA	18
22 - 23	2	Design for Performance	€ 1600 + IVA	18
27 - 28	2	Minimizing Your Design Time with the ChipScope Pro Debug and Verification Tools	€ 1600 + IVA	18

Novembre 2012

L	M	M	G	V	S	D
			1	2	3	4
5	**6**	**7**	8	9	10	11
12	13	14	**15**	**16**	17	18
19	**20**	21	**22**	**23**	24	25
26	**27**	**28**	29	30		

Data (*)	Durata	Corso	Costo	TC
3 - 4 - 5	3	Designing with VHDL	€ 1800 + IVA	21
10 - 11	2	Embedded Systems Development	€ 1600 + IVA	18
13 - 14	2	DSP Design Using System Generator	€ 1600 + IVA	18
18 - 19	2	Advanced FPGA Implementation	€ 1600 + IVA	18

Dicembre 2012

L	M	M	G	V	S	D
					1	2
3	**4**	**5**	6	7	8	9
10	**11**	12	**13**	**14**	15	16
17	**18**	**19**	20	21	22	23
24	25	26	27	28	29	30
31						

(*) Mindway si riserva il diritto di modificare le date o di cancellare i corsi già pianificati in caso di insufficiente numero di iscritti.

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